IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Lance Flake	
Appln. No.:	10/801,209	Group Art Unit: 2113
Filed :	March 16, 2004	
For :	METHODS AND STRUCTURE FOR ERROR CORRECTION IN PROCESSOR PIPELINE	Examiner: Wilson
Docket No.:	M142.12-0029	

RESPONSE

I HEREBY CERTIFY THAT THIS PAPER IS BEING SENT BY U.S. MAIL, FIRST CLASS, TO THE COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, THIS

12th DAY OF April, 2007.

PATENT ATTORNEY

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Commissioner for Patents
P.O. Box 1450
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Sir:

This is in response to the Office Action mailed on January 12, 2007 and the telephonic interview held between the Examiner and the undersigned attorney on April 5, 2007. In the Office Action, all claims 1-29 were rejected. With this response, no claims are amended and all claims are presented for reconsideration and allowance.

Section Two of the Office Action indicated that independent claims 1 and 17, among others, were rejected under 35 U.S.C. §102(b) as being anticipated by Bauer et al. (U.S. Patent 5,604,753 - hereinafter Bauer). Applicant respectfully traverses this rejection in view of the following.

Independent 1 provides, among other things, a processor having a memory interface comprising a multi-stage pipeline for fetching or reading information from a memory coupled to the processor. The pipeline is further defined to include, among other things, a correction stage to correct a soft error detected in a read unit of information. Similarly, independent claim 17 provides a method for correcting soft errors in a pipeline processor coupled to a memory subsystem. The method includes, among other things, correcting a soft error in the

read information in a correction stage of the processor pipeline. Applicant respectfully believes that the Office Action has not given proper effect to the claim language directed to the pipelined processor, as well as the correction stage.

Section Two of the Office Action asserts, "As per claims 1, 17, Bauer et al. discloses a multi-stage pipeline for fetching or reading information from a memory coupled to the processor, see Figure 6, the pipeline including ... a correction stage to correct a soft error detected in a read unit of information in column 6, lines 17-34...."

As a threshold matter, it is important for proper meaning to be given to the term "pipeline" in the claim language. At least one resource reports that, in the context of computing, a "Pipeline" is a set of data processing elements connected in series, so that the output of one element is the input of the next one." See Pipeline (computer), http://en.wikipeda.org/w/index/php?title=Pipeline_%28computer%29&oldid=105423028 (last visited February 15, 2007). Accordingly, in the current context, the recitation of the "pipeline" limitation requires multiple stages where the output of one stage is the input of a next one. This is important because Bauer, in providing a method and apparatus for performing error correction on data from an external memory (see Title), does so in a deliberate non-pipelined manner. For example, column 5, lines 55-59 provide,

> "In the present invention, the desired data returned is sent directly to execution core 101A for immediate use, while the error correction is performed in parallel by ECC logic 101C. Thus the present invention bypasses the data directly to the execution core 101A without error correction initially." (Emphasis supplied).

Accordingly, Applicant respectfully believes that the teachings of Bauer are precisely the opposite of the pipeline features recited in claims 1 and 17. This is further evident when considering the alleged elements of Bauer that are asserted as reading upon the elements of independent claims 1 and 17.

Section Two of the Office Action asserted that Bauer discloses a multi-stage pipeline for fetching or reading information from a memory coupled to the processor as indicated in FIG. 6. FIG. 6 of Bauer, however, is merely a block diagram of execution core 503 (shown in FIG. 5). The alleged read stage of Bauer apparently is provided in column 11, lines 21-34.

However, that disclosure is directly to instruction fetch and issue unit 501, which works cooperatively with execution core 503. Accordingly, element 501 is not a sub-component of execution core 503, as the read stage set forth in independent claims 1 and 17 is a sub-component of the processor pipeline. Further still, the correction stage is asserted, by the Office Action, to be met by disclosure in Bauer at column 6, lines 17-34. However, the cited portion only speaks of the data path between the L2 cache memory and the processor. Specifically, the description therein refers to data correction block 204 and data correction block 216. However, there does not appear to be any indication that either data correction blocks 204 or 216 are anything that would be equivalent to a correction stage of a pipelined processor. Further still, there is simply no indication that block 204 and/or 216 are sub-components of execution core 503, asserted by Section Two of the Office Action as being the multi-stage pipeline for fetching or reading information from a memory coupled to the processor.

Accordingly, Applicant respectfully submits that independent claims 1 and 17 are neither taught nor suggested by Bauer. Additionally, Applicant respectfully submits that dependent claims 2-16 and 18-29 are allowable as well by virtue of their dependency, either directly or indirectly, from allowable independent claims.

In conclusion, Applicant respectfully submits that the entire application is now in condition for allowance. Reconsideration and favorable action are respectfully requested.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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